AMENDMENTS TO THE CLAIMS

Please replace all prior versions of the claims with the following claim listing:

Claims:

1. (Previously Presented) A method for generating a set of test vectors for testing an integrated circuit, each test vector of the set of test vectors containing a plurality of bits defining test inputs for the integrated circuit, the method comprising the steps of:

defining a list of faults for the integrated circuit;

generating at least one test vector that defines values for those inputs necessary to detect at least one target fault selected from the list of faults, the values comprising only a portion of the bits of the at least one test vector, wherein a remainder of the bits in the at least one test vector are unspecified bit positions; and

setting the values of a plurality of the unspecified bit positions using a non-random filling methodology.

2. (Original) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions to a value of one.

3. (Original) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions to a value of zero.

4. (Original) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes extending a value of a last specified bit position to set a plurality of the unspecified bit positions to a value equal to the last specified bit position.

5. (Original) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes setting each of the plurality of the unspecified bit positions using a repeating pattern of ones and zeros.

6. (Currently Amended) The method as defined in claim 1, wherein the step of setting the values of the unspecified bit positions includes ~~setting each of the plurality of the unspecified bit positions using an algorithm that is conducive to compression~~ using an algorithm to set the plurality of unspecified bit positions of the at least one test vector such that the at least one test vector can be compressed.

7. (Currently Amended) The method as defined in claim 1, further including the step of setting a second plurality of the unspecified bit positions in accordance with a random filling methodology.

8. (Previously Presented) The method as defined in claim 1, further including the steps of:

adding a first test vector to a list of test vectors and marking the selected fault as detected;

generating an additional test vector which defines values for those inputs necessary to detected a target fault selected from the list of faults, and other than one marked as detected;

determining whether the additional test vector may be compacted with any test vector in the list of test vectors, and if so, compacting the additional test vector with a test vector in the set of test vectors, and if not, adding the additional test vector to the set of test vectors.

9. (Previously Presented) The method as defined in claim 1, wherein a first test vector of the plurality of test vectors defines values for those inputs necessary to detect a plurality of target faults selected from the list of faults.

10. (Previously Presented) The method as defined in claim 1, wherein additional test vectors of the plurality of test vectors define values for those inputs necessary to detect a plurality of target faults selected from the list of faults.

11. (Previously Presented) The method as defined in claim 1, wherein a first test vector of the plurality of test vectors defines values for only those inputs necessary to detect a target fault selected from the list of faults.

12. (Previously Presented) The method as defined in claim 1, further including the step of fault simulating a first test vector created in the generating step to determine if the first test vector detects additional faults, and if so, marking said additional faults as detected.

13. (Original) The method as defined in claim 1, wherein the integrated circuit is a portion of a larger integrated circuit chip.

14. (Previously Presented) The method as defined in claim 1, wherein outputs for the at least one test vector are generated in response to the compacted condition.

15. (Previously Presented) An apparatus for generating a set of test vectors comprising:

first means for evaluating a list of faults and generating at least one test vector configured to test at least one fault on the list of faults, the at least one test vector defining values for those inputs necessary to detect at least one target fault selected from the list of faults, the values comprising only a portion of the bits of the at least one test vector, wherein a remainder of the bits in the at least one test vector are unspecified bit positions; and

second means for setting a plurality of the values of the unspecified bit positions using a non-random filling methodology.

16. (Previously Presented) The apparatus as defined in claim 15, wherein the second means sets the values of the unspecified bit positions by setting each of the unspecified bit positions to a value of one.

17. (Previously Presented) The apparatus as defined in claim 15, wherein the second means sets the values of the unspecified bit positions by setting each of the unspecified bit positions to a value of zero.

18. (Previously Presented) The apparatus as defined in claim 15, wherein the second means sets the values of the unspecified bit positions by setting each of the unspecified bit positions to a repeating pattern of ones and zeros.

19. (Currently Amended) The apparatus as defined in claim 15, wherein the ~~step of setting~~ second means sets the values of the unspecified bit positions ~~includes~~ by extending a value of a last specified bit position to set a plurality of the unspecified bit positions to a value equal to the last specified bit position.

20. (Currently Amended) The apparatus as defined in claim 15, wherein the ~~step of setting~~ second means sets the values of the unspecified bit positions ~~includes setting each of the plurality of the unspecified bit positions using an algorithm that is conducive to compression~~ by using an algorithm to set the plurality of unspecified bit positions of the at least one test vector such that the at least one test vector can be compressed.

21. (New) The method as defined in claim 6, further comprising the step of compressing the at least one test vector.

22. (New) The apparatus as defined in claim 20, further comprising means for compressing the at least one test vector.